EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	89	(Whay near Lee).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:46
L2	16	(walter near Nixon).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:46
L3	0	(Chong near "Jr.").in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:46
L4	27744	"711"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:48
L5	24294261	@ad<"20030717"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:49
L6	19421	shared adj memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:49
L7	2052303	synchronous$4 or simultaneous$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:49
L8	2169630	switch$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:49
L9	43064	memory adj (bank$2 or module$2 or segment$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:50

EAST Search History

L10	350297	multiplex$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:50
L11	1869	rotat$4 adj selector$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:51
L12	214	successive adj clock adj cycle	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:51
L13	0	ratchering adj distributor$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:52
L14	1	ratcheting adj distributor$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:52
L15	102	1 or 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:52
L16	23915	4 and 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:52
L17	11416	7 and 8 and 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:53
L18	1454	16 and 17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:53
L19	847	18 and 10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:53

EAST Search History

L20	2	19 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/01 10:53

Terms used
shared memory switch multiplexer selector bank module segment

Found **38** of **169,866**

Sort results by: relevance
Display results: expanded form
Save results to a Binder
Search Tips
Open results in a new window

Try an Advanced Search
Try this search in The ACM Guide

Results 1 - 20 of 38 Result page: **1** 2 next

Relevance scale

1 Multiple instruction issue in the NonStop cyclone processor

Robert W. Horst, Richard L. Harris, Robert L. Jardine
May 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual international symposium on Computer Architecture ISCA '90**, Volume 18 Issue 3a
Publisher: ACM Press

Full text available: pdf(1.06 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the architecture for issuing multiple instructions per clock in the NonStop Cyclone Processor. Pairs of instructions are fetched and decoded by a dual two-stage prefetch pipeline and passed to a dual six-stage pipeline for execution. Dynamic branch prediction is used to reduce branch penalties. A unique microcode routine for each pair is stored in the large duplexed control store. The microcode controls parallel data paths optimized for executing the most frequent instr ...

2 Curriculum 68: Recommendations for academic programs in computer science: a report of the ACM curriculum committee on computer science

William F. Atchison, Samuel D. Conte, John W. Hamblen, Thomas E. Hull, Thomas A. Keenan, William B. Kehl, Edward J. McCluskey, Silvio O. Navarro, Werner C. Rheinboldt, Earl J. Schweppe, William Viavant, David M. Young
March 1968 **Communications of the ACM**, Volume 11 Issue 3
Publisher: ACM Press
Full text available: pdf(6.63 MB) Additional Information: full citation, references, citings

Keywords: computer science academic programs, computer science bibliographies, computer science courses, computer science curriculum, computer science education, computer science graduate programs, computer science undergraduate programs

3 A reconfigurable hardware approach to network simulation

Dimitrios Stiliadis, Anujan Varma
January 1997 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 7 Issue 1
Publisher: ACM Press

Additional Information:

Full text available: pdf(925.18 KB) full citation, references, citings, index terms, review

Keywords: ATM switch scheduling, field-programmable gate array, hardware simulation

4 ATM Architectures Using Optical Technology: An Overview of Switching, Buffering and Multiplexing

M. Guizani

July 1997 **International Journal of Network Management**, Volume 7 Issue 4

Publisher: John Wiley & Sons, Inc.

Full text available: pdf(525.89 KB) Additional Information: full citation, abstract, references, index terms

This overview presents recent studies on photonic switches and discusses the existing different types, such as space-division switches, free-space switches, time-division switches, wavelength division switches, and frequency division switches. The architectures and applications of these switches are also discussed. © 1997 John Wiley & Sons, Ltd.

5 Computer communication techniques

Kenneth J. Thurber

October 1978 **ACM SIGARCH Computer Architecture News**, Volume 7 Issue 3

Publisher: ACM Press

Full text available: pdf(1.26 MB) Additional Information: full citation, abstract, references

This paper examines the concept of computer communication systems as seen from the viewpoint of the system architectures of distributed processor systems and networks. The fundamental concepts of bus structures, circuit switches, and message/packet switches are examined.

6 ARPS: a new real-time computer

Kenneth J. Thurber

October 1976 **ACM SIGARCH Computer Architecture News**, Volume 5 Issue 4

Publisher: ACM Press

Full text available: pdf(1.14 MB) Additional Information: full citation, references, citings

7 Reducing power in superscalar processor caches using subbanking, multiple line buffers and bit-line segmentation

Kanad Ghose, Milind B. Kamble

August 1999 **Proceedings of the 1999 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: pdf(789.43 KB) Additional Information: full citation, references, citings, index terms

Keywords: low power caches, power estimation

8 A hardware laboratory for computer architecture research

Jean Vaucher, Christian Rey

December 1973 **ACM SIGARCH Computer Architecture News , Proceedings of the 1st annual symposium on Computer architecture ISCA '73**, Volume 2 Issue 4

Publisher: ACM Press

Full text available: pdf(518.91 KB) Additional Information: full citation, abstract, references, citings, index terms

Because of dramatic reductions in cost of mini-computers, peripherals and logic modules, it is becoming evident that many problems confronting the computer system designer will be solved in the future by hybrid designs involving not only software but also specialized computers with architectures best suited to each application. Accordingly, hardware research must no longer be considered as a separate discipline by system programmers but as a tool in exactly the same way as languages. To ill ...

9 Architecture of the IBM system/370

Richard P. Case, Andris Padegs
January 1978 **Communications of the ACM**, Volume 21 Issue 1
Publisher: ACM Press

Full text available: pdf(2.78 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper discusses the design considerations for the architectural extensions that distinguish System/370 from System/360. It comments on some experiences with the original objectives for System/360 and on the efforts to achieve them, and it describes the reasons and objectives for extending the architecture. It covers virtual storage, program control, data-manipulation instructions, timing facilities, multiprocessing, debugging and monitoring, error handling, and input/output operations. ...

Keywords: architecture, computer systems, error handling, instruction sets, virtual storage

10 STEP development tools: METASTEP language system

D. L. Wilburn, S. Schleimer
December 1985 **ACM SIGMICRO Newsletter , Proceedings of the 18th annual workshop on Microprogramming MICRO 18**, Volume 16 Issue 4
Publisher: ACM Press

Full text available: pdf(789.53 KB) Additional Information: full citation, abstract, references, index terms

STEP Development Tools (SDT) is a general-purpose microprogram development system. The METASTEP language system is composed of four tools of the SDT needed to write microprograms: a Definition Processor, a Retargetable Assembler, a Retargetable Cross-Assembler, and a Relocatable Linker. These tools are of commercial quality, providing complete languages, quality diagnostics, full interface to other support tools, and high performance. The language system supports microcode debug ...

11 Designing SoCs for yield improvement: Using embedded FPGAs for SoC yield improvement

Miron Abramovici, Charles Stroud, Marty Emmert
June 2002 **Proceedings of the 39th conference on Design automation**
Publisher: ACM Press

Full text available: pdf(200.31 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we show that an embedded FPGA core is an ideal host to implement infrastructure IP for yield improvement in a bus-based SoC. We present methods for testing, diagnosing, and repairing embedded FPGAs, for which complete testability is achieved without any area overhead or performance degradation. We show how an FPGA core can provide embedded testers for other cores in the SoC, so that cores designed to be tested with external vectors can be tested with BIST, and the entire SoC can be ...

12 Fowarding: Scaling internet routers using optics

Isaac Keslassy, Shang-Tse Chuang, Kyoungsik Yu, David Miller, Mark Horowitz, Olav Solgaard, Nick McKeown

August 2003 **Proceedings of the 2003 conference on Applications, technologies, architectures, and protocols for computer communications**

Publisher: ACM Press

Full text available: pdf(253.06 KB) Additional Information: full citation, abstract, references, index terms

Routers built around a single-stage crossbar and a centralized scheduler do not scale, and (in practice) do not provide the throughput guarantees that network operators need to make efficient use of their expensive long-haul links. In this paper we consider how optics can be used to scale capacity and reduce power in a router. We start with the promising load-balanced switch architecture proposed by C-S. Chang. This approach eliminates the scheduler, is scalable, and guarantees 100% throughput f ...

Keywords: internet router, load-balancing, packet-switch

13 Concurrent analysis techniques for data path timing optimization

Chuck Monahan, Forrest Brewer

June 1996 **Proceedings of the 33rd annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(76.54 KB) Additional Information: full citation, references, citings, index terms

14 A Measurement Procedure for Queueing Network Models of Computer Systems

Clifford A. Rose

September 1978 **ACM Computing Surveys (CSUR)**, Volume 10 Issue 3

Publisher: ACM Press

Full text available: pdf(1.70 MB) Additional Information: full citation, references, citings, index terms

15 The UniMIN switch architecture for large-scale ATM switches

Sung Hyuk Byun, Dan Keun Sung

February 2000 **IEEE/ACM Transactions on Networking (TON)**, Volume 8 Issue 1

Publisher: IEEE Press

Full text available: pdf(283.61 KB) Additional Information: full citation, references, index terms

Keywords: ATM switch, UniMIN, distribution network, fair virtual FIFO, general expansion architecture

16 The Personal Presence System—hardware architecture

M. Lukacs

October 1994 **Proceedings of the second ACM international conference on Multimedia**

Publisher: ACM Press

Full text available: pdf(957.84 KB) Additional Information: full citation, abstract, references, citings, index terms

The Personal Presence System (PPS) experimental prototype is being designed to support multiparty multimedia visual services which use advanced video combining techniques.

This paper is a companion to another paper in this proceedings: "The Personal Presence System—A Wide Area Network Service Resource for the Real Time Composition of Multipoint Multimedia Communications" which contains a detailed service description.This paper describes the architecture of the A ...

17 Transaction papers: Flexible bandwidth allocation in high-capacity packet switches

Aleksandra Smiljanić
April 2002 **IEEE/ACM Transactions on Networking (TON)**, Volume 10 Issue 2
Publisher: IEEE Press
Full text available: pdf(259.14 KB) Additional Information: full citation, abstract, references, index terms

This paper introduces a protocol for scheduling of packets in high-capacity switches, termed weighted sequential greedy scheduling (WSGS). WSGS is a simple, greedy algorithm that uses credits to reserve bandwidth for input-output pairs. By using a pipeline technique, WSGS implemented by the current technology readily supports a switching capacity exceeding 1 Tb/s. Admission control is straightforward, allowing bandwidth reservations on a submillisecond time scale. Namely, the central controller ...

Keywords: packet switching, scalability, scheduling, switch with input buffers

18 The modeling and synthesis of bus systems

Chia-Jeng Tseng, Daniel P. Siewiorek
June 1981 **Proceedings of the 18th conference on Design automation**
Publisher: IEEE Press
Full text available: pdf(629.38 KB) Additional Information: full citation, abstract, references, citings, index terms

A bus oriented interconnection of registers and data operators is the dominant mode of design for the data paths of digital systems. A study of ten processor implementations, ranging in size from microprocessors to large mainframes, spanning almost 20 years in the practice of digital design, indicated a strong similarity. From this study bus style primitives and generic bus models were developed. The generic bus models were simplified to match each of the ten processors composing the study. ...

19 A virtual machine emulator for performance evaluation

M. D. Canon, D. H. Fritz, J. H. Howard, T. D. Howell, M. F. Mitoma, J. Rodriquez-Rosell
February 1980 **Communications of the ACM**, Volume 23 Issue 2
Publisher: ACM Press
Full text available: pdf(865.59 KB) Additional Information: full citation, references, citings

Keywords: computer system simulation, performance evaluation, virtual machines

20 An interactive design automation system

Stephen Y. H. Su
June 1973 **Proceedings of the 10th workshop on Design automation**
Publisher: IEEE Press
Full text available: pdf(851.96 KB) Additional Information: full citation, abstract, references, citings, index terms

An interactive design automation system is presented which, after complete implementation, will allow the designer to check the determinacy and dead locks of the system before implementation. The design can be evaluated at various levels and modified

interactively. The designer enters his design specification using either graphical representation or design language statements. The translator accepts the input and produces a data base for both the simulator and the logic synthesizer. The syn ...

Results 1 - 20 of 38 Result page: **1** 2 next

Wed, 1 Feb 2006, 11:01:00 AM EST

Edit an existing query or compose a new query in the Search Query Display.

Select a search number (#) to:

- Add a query to the Search Query Display
- Combine search queries using AND, OR, or NOT
- Delete a search
- Run a search

Search Query Display

[redacted]

Recent Search Queries

#1	((shared memory)<in>metadata)
#2	(switches or switch<IN>metadata)
#3	(synchronously or simultaneously<IN>metadata)
#4	(successive cycle<IN>metadata)
#5	(synchronously or simultaneously<IN>metadata)
#6	(rotating selector<IN>metadata)
#7	(ratcheting distributor<IN>metadata)
#8	(((shared memory)<in>metadata)) <AND> ((switches or switch<IN>metadata))
#9	((((shared memory)<in>metadata)) <AND> ((switches or switch<IN>metadata))) <AND> ((successive cycle<IN>metadata))
#10	((switches or switch<IN>metadata)) <AND> ((synchronously or simultaneously<IN>metadata))
#11	((((shared memory)<in>metadata)) <AND> ((switches or switch<IN>metadata))) <AND> (((switches or switch<IN>metadata)) <AND> ((synchronously or simultaneously<IN>metadata)))

[redacted]